

THYRISTOR MODULE

133A / 800V

P A T 6 0 8

P A H 6 0 8

FEATURES

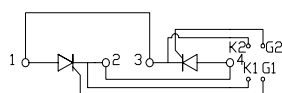
- * Isolated Base
- * Dual Thyristors or Thyristor and Diode Anti-Parallel Circuit
- * High Surge Capability
- * UL Recognized, File No. E187184

TYPICAL APPLICATIONS

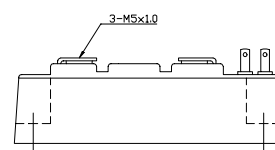
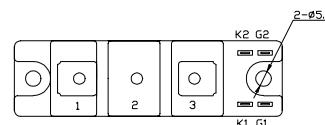
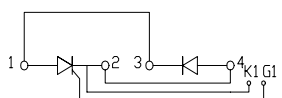
- * AC phase control
- * AC switch

OUTLINE DRAWING

PAT



PAH



Maximum Ratings

Approx Net Weight:155g

Parameter	Symbol	Grade	Unit
		PAT/PAH608	
Repetitive Peak Off-State Voltage	V_{DRM}	800	V
Non Repetitive Peak Off-State Voltage	V_{DSM}	960	

Parameter		Conditions	Max Rated Value	Unit
RMS On-State Current	$I_{T(RMS)}$	50Hz Half Sine Wave condition $T_c=83^{\circ}C$	133	A
Surge On-State Current	I_{FSM}	50 Hz Half Sine Wave, 1Pulse Non-Repetitive	1200	A
I Squared t	I^2t	2msec to 10msec	7200	A ² s
Critical Rate of Turned-On Current	di/dt	$V_D=2/3V_{DRM}$, $I_{TM}=2 \cdot I_O$, $T_j=125^{\circ}C$ $I_G=200mA$, $di_G/dt=0.2A/\mu s$	100	A/ μs
Peak Gate Power	P_{GM}		5	W
Average Gate Power	$P_{G(AV)}$		1	W
Peak Gate Current	I_{GM}		2	A
Peak Gate Voltage	V_{GM}		10	V
Peak Gate Reverse Voltage	V_{RGM}		5	V
Operating Junction Temperature Range	T_{jw}		-40 to +125	$^{\circ}C$
Storage Temperature Range	T_{stg}		-40 to +125	$^{\circ}C$
Isolation Voltage	Viso	Base Plate to Terminals, AC1min	2000	V
Mounting torque	Case mounting	Ftor	M5 Screw	N.m
	Terminals		M5 Screw	

Value per 1 Arm

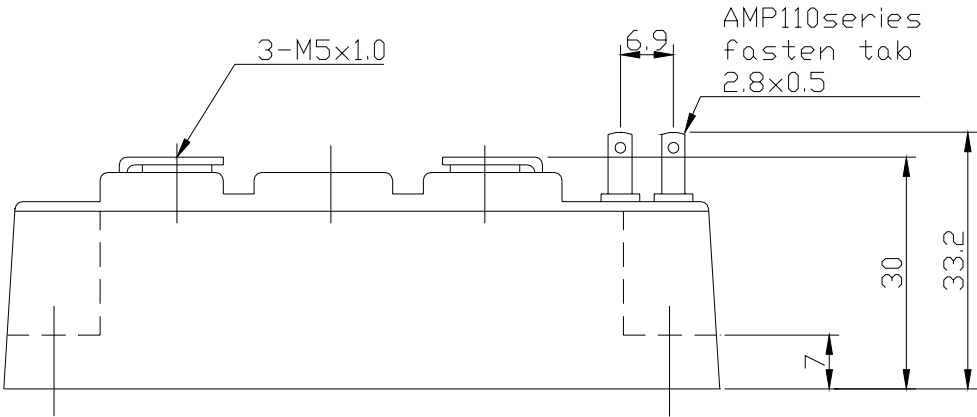
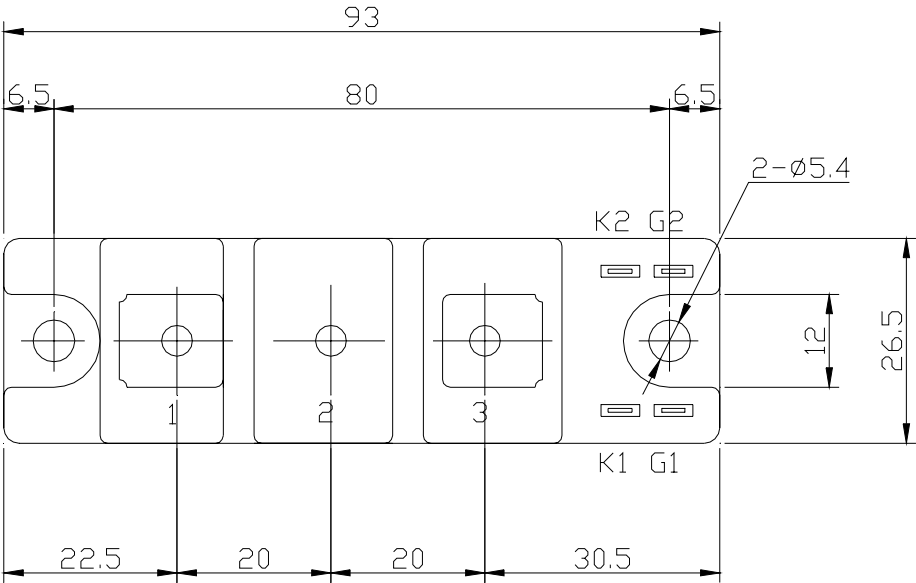
Electrical • Thermal Characteristics

Characteristics	Symbol	Test Conditions	Maximum Value.			Unit
			Min.	Typ.	Max.	
Peak Off-State Current	I_{DM}	$V_{DM} = V_{DRM}, T_j = 125^{\circ}C$			30	mA
Peak On-State Voltage	V_{TM}	$I_{TM} = 180A, T_j = 25^{\circ}C$			1.38	V
Gate Current to Trigger	I_{GT}	$V_D = 6V, I_T = 1A$			200	mA
					100	
					50	
Gate Voltage to Trigger	V_{GT}	$V_D = 6V, I_T = 1A$			4	V
					2.5	
					2	
Gate Non-Trigger Voltage	V_{GD}	$V_D = 2/3V_{DRM}, T_j = 125^{\circ}C$	0.25			V
Critical Rate of Rise of Off-State Voltage	dv/dt	$V_D = 2/3V_{DRM}, T_j = 125^{\circ}C$	500			V/ μs
Turn-Off Time	t_q	$I_{TM} = I_o, V_D = 2/3V_{DRM}$ $dv/dt = 20V/\mu s, V_R = 100V$ $-di/dt = 20A/\mu s, T_j = 125^{\circ}C$		100		μs
Turn-On Time	t_{gt}	$T_j = 25^{\circ}C, I_{TM} = I_{T(RMS)}$		6		μs
Delay Time	t_d	$V_D = 100V, I_G = 200mA$		2		μs
Rise Time	t_r	$di_G/dt = 0.2A/\mu s$		4		μs
Latching Current	I_L	$T_j = 25^{\circ}C$		100		mA
Holding Current	I_H	$T_j = 25^{\circ}C$		50		
Thermal Resistance *1	$R_{th(j-c)}$	Junction to Case			0.25	$^{\circ}C/W$
	$R_{th(c-f)}$	Base Plate to Heat Sink with Thermal Compound			0.1	

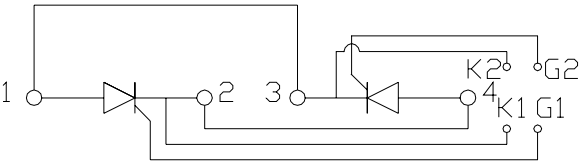
Value Per 1Arm

*1: Value Per Module

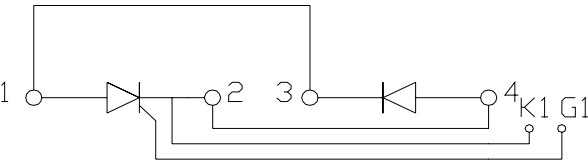
PAT/PAH608 OUTLINE DRAWING (Dimensions in mm)



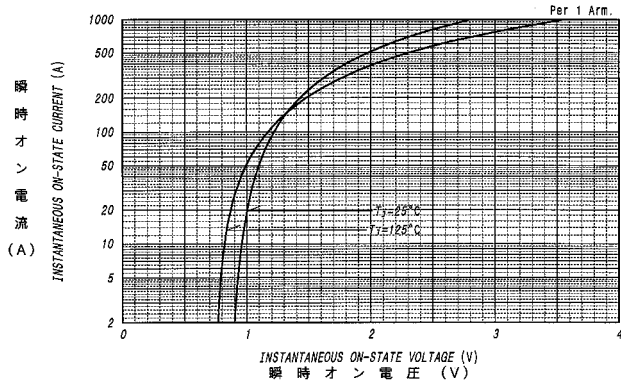
PAT



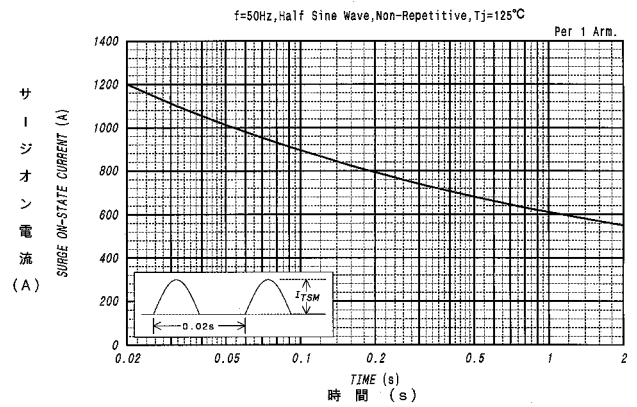
PAH



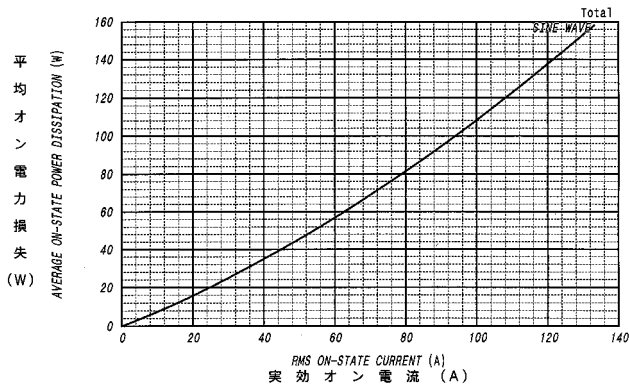
オン電圧特性
ON-STATE CURRENT VS. VOLTAGE



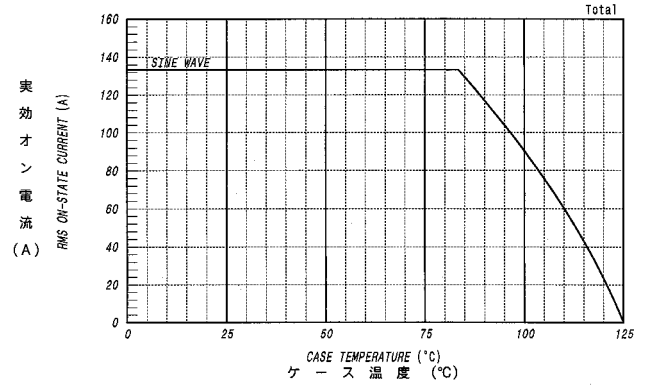
サージオン電流定格
SURGE CURRENT RATINGS



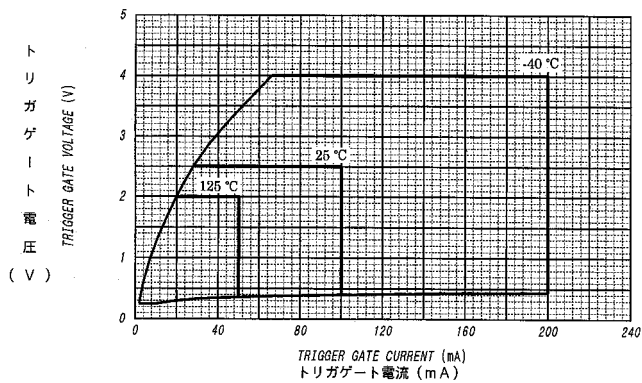
平均オン電力損失特性
AVERAGE ON-STATE POWER DISSIPATION



実効オン電流-ケース温度定格
RMS ON-STATE CURRENT VS. CASE TEMPERATURE



ゲート特性
GATE CHARACTERISTICS



ゲート定格
GATE RATINGS

