

SKM 100GB124D



SEMITRANS™ 2

Low Loss IGBT Module

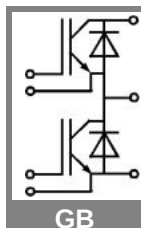
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Features

- MOS input (voltage controlled)
- N channel, homogeneous Silicon structure (NPT- Non punch-through IGBT)
- Low loss high density chip
- Low tail current
- High short circuit capability, self limiting to $6 \times I_{Cnom}$
- Latch-up free
- Fast & soft inverse CAL diodes
- Isolated copper baseplate using DCB Direct Copper Bonding Technology without hard mould
- Large clearance (10 mm) and creepage distances (20 mm)

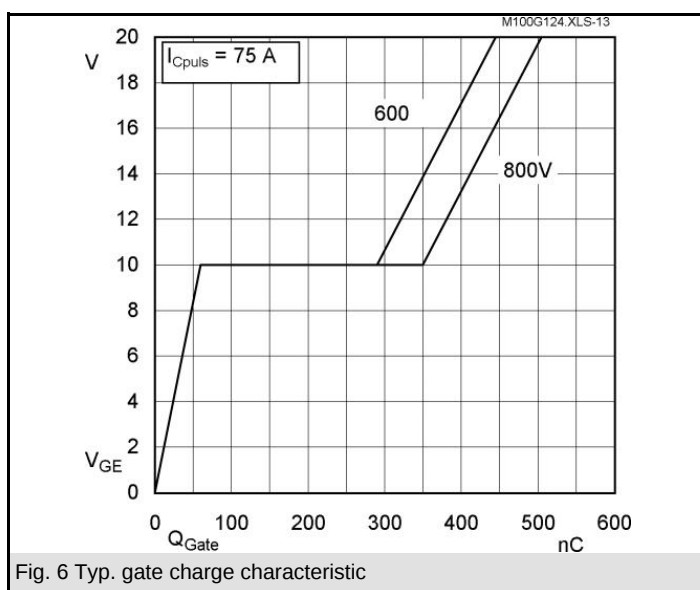
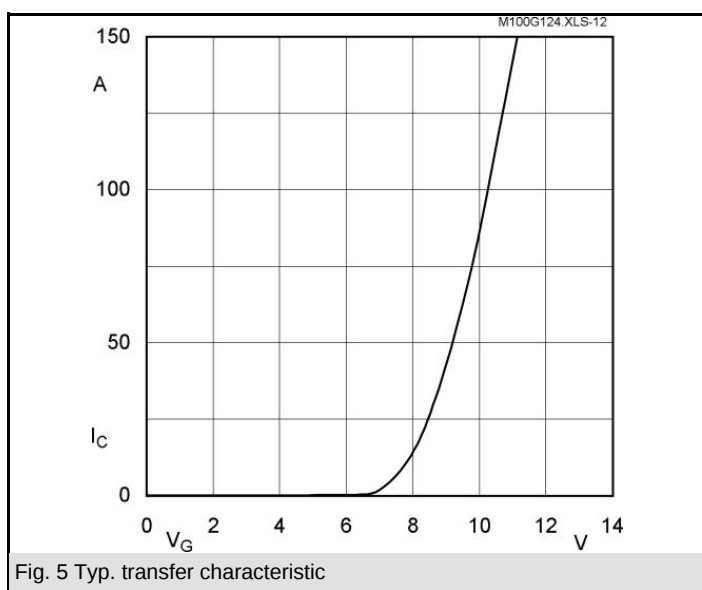
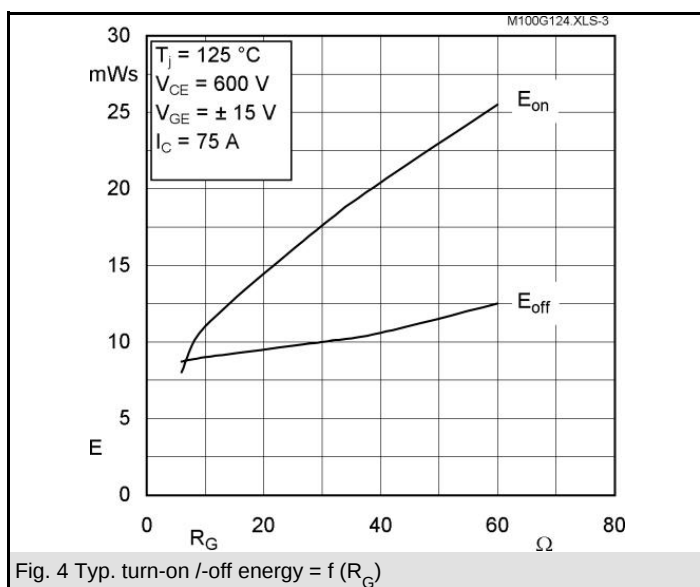
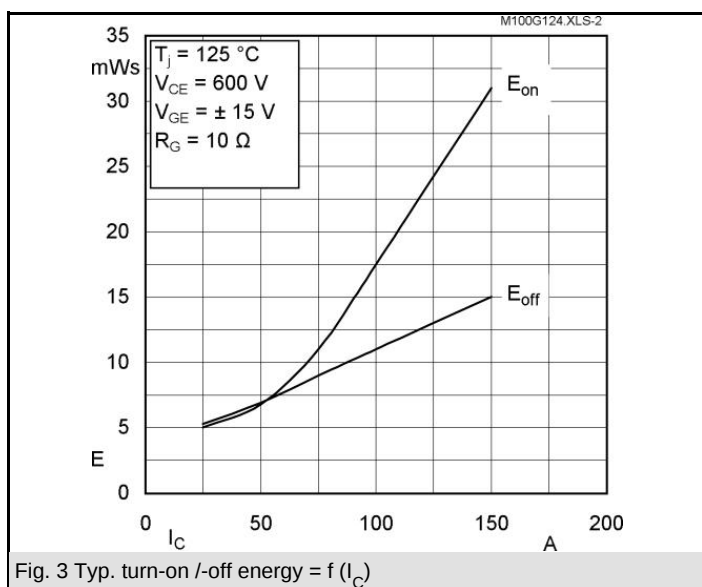
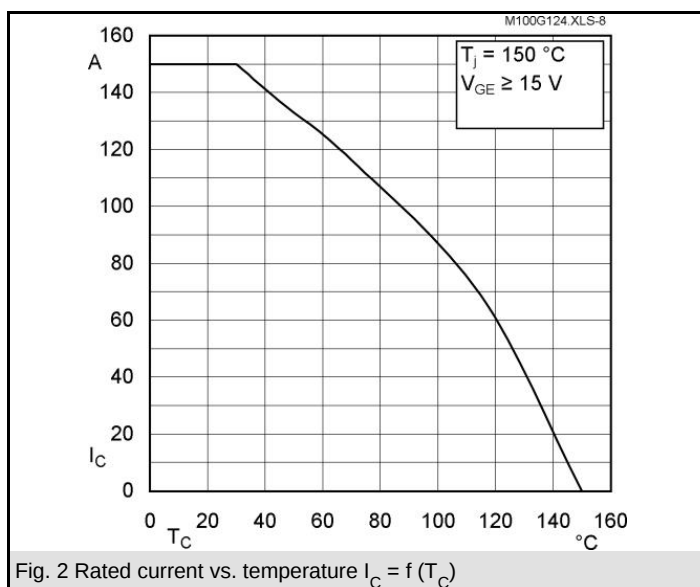
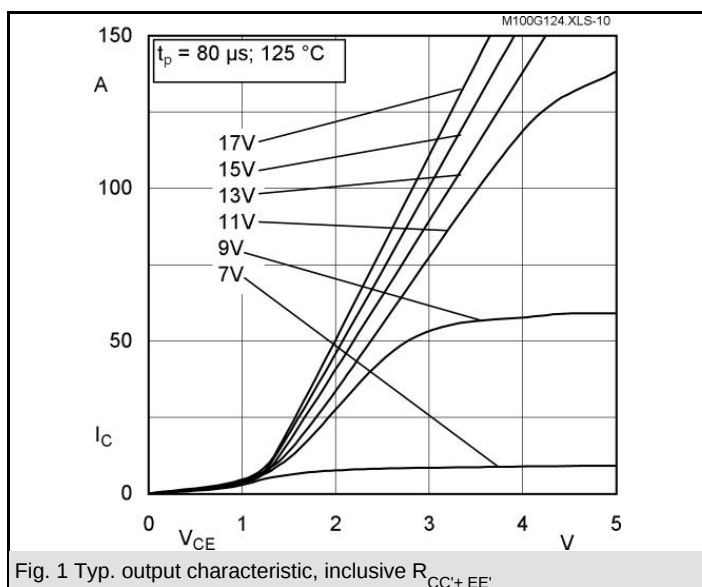
Typical Applications

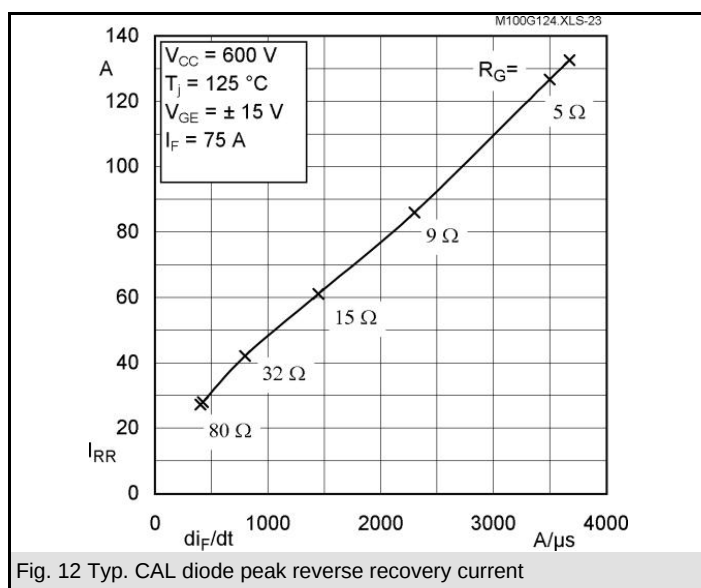
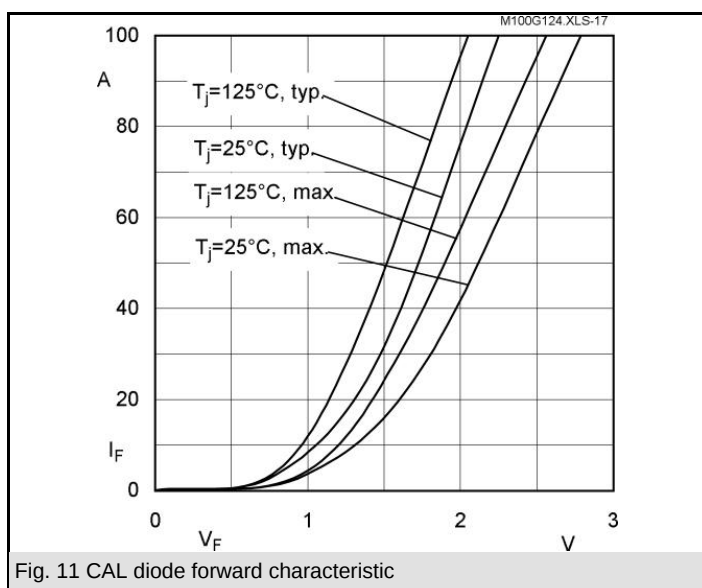
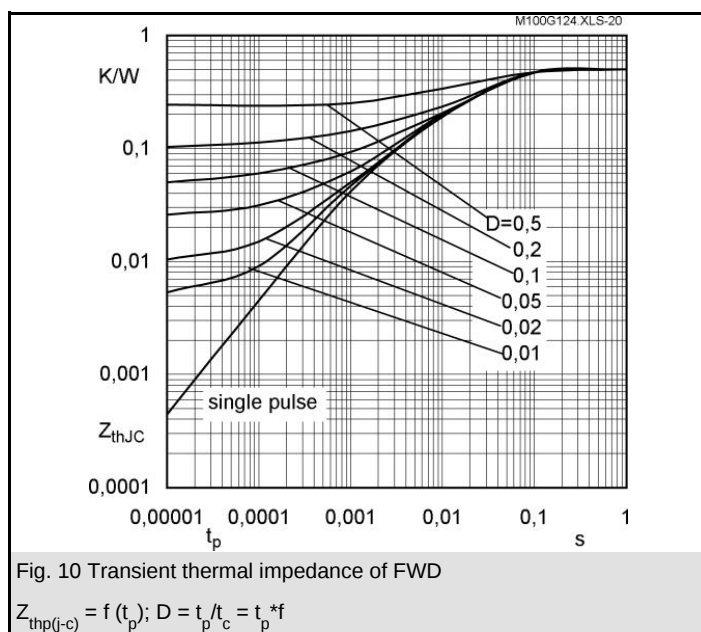
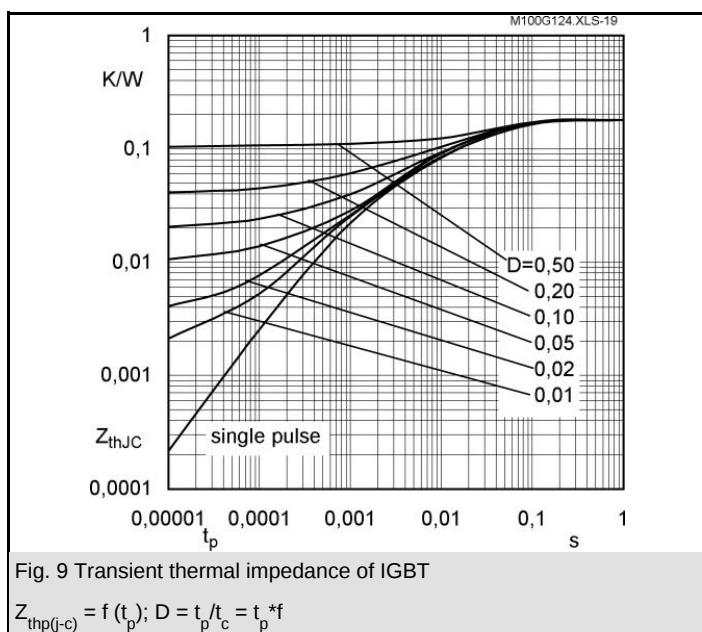
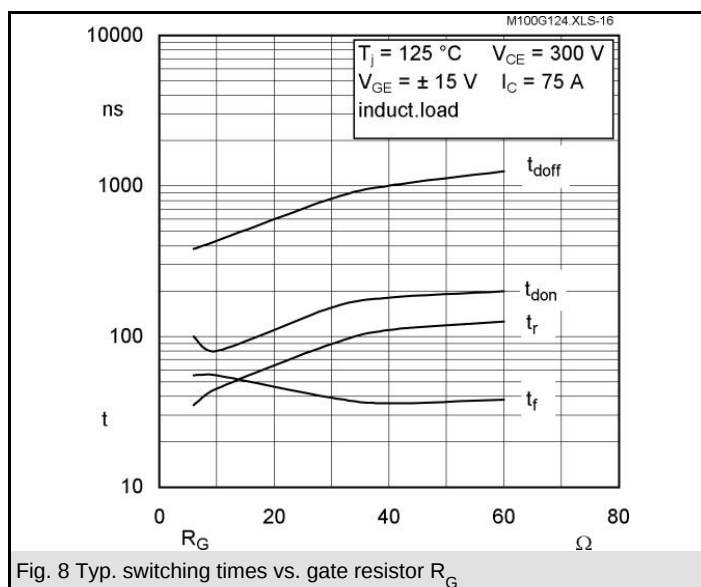
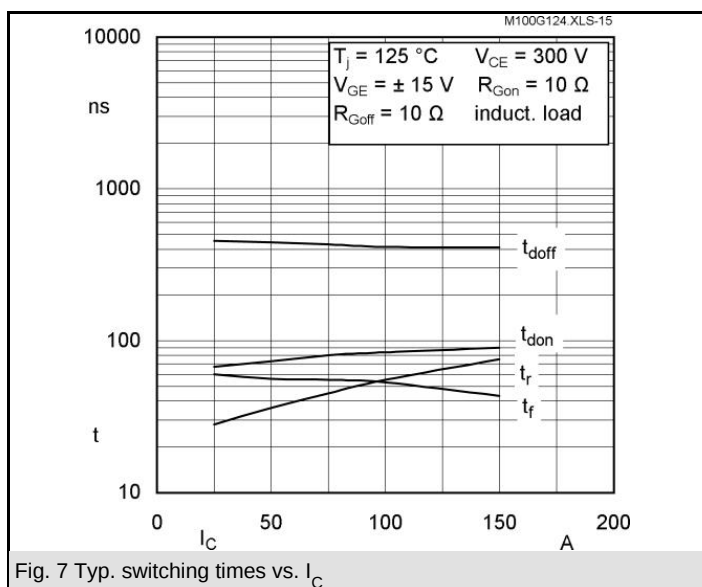
- Switching (not for linear use)

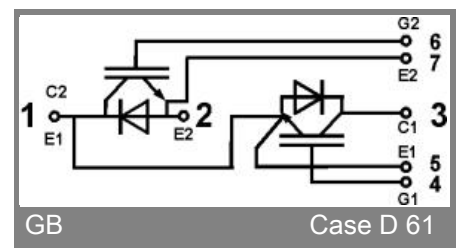
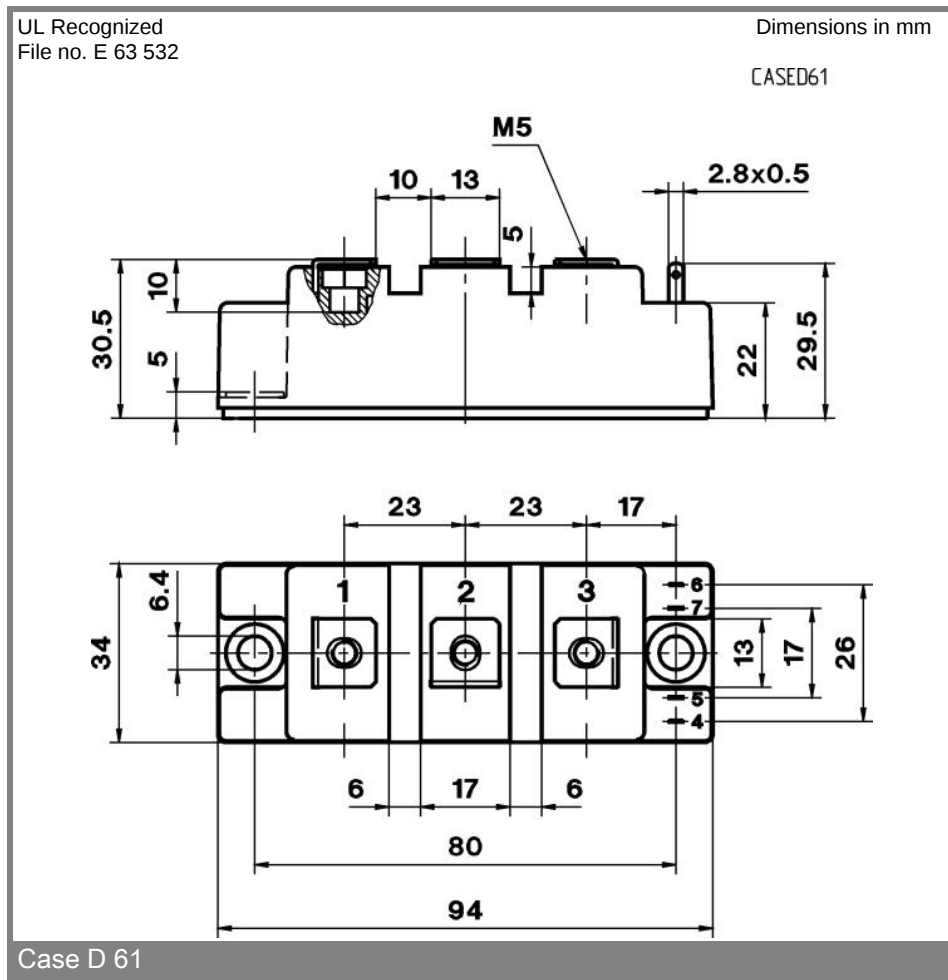
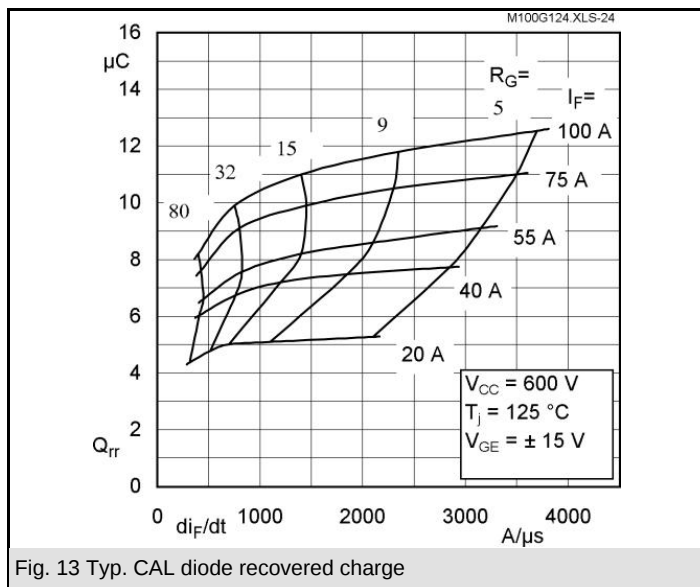


Absolute Maximum Ratings		$T_c = 25^\circ\text{C}$, unless otherwise specified	
Symbol	Conditions	Values	Units
IGBT			
V_{CES}		1200	V
I_C	$T_c = 25 (85)^\circ\text{C}$	150 (100)	A
I_{CRM}	$t_p = 1 \text{ ms}$	150	A
V_{GES}		± 20	V
T_{vj} (T_{stg})	$T_{OPERATION} \leq T_{stg}$	- 40 ... + 150 (125)	$^\circ\text{C}$
V_{isol}	AC, 1 min.	2500	V
Inverse diode			
I_F	$T_c = 25 (80)^\circ\text{C}$	95 (65)	A
I_{FRM}	$t_p = 1 \text{ ms}$	150	A
I_{FSM}	$t_p = 10 \text{ ms}$; sin.; $T_j = 150^\circ\text{C}$	720	A

Characteristics		$T_c = 25^\circ\text{C}$, unless otherwise specified			
Symbol	Conditions	min.	typ.	max.	Units
IGBT					
$V_{GE(th)}$	$V_{GE} = V_{CE}$, $I_C = 2 \text{ mA}$	4,5	5,5	6,5	V
I_{CES}	$V_{GE} = 0$, $V_{CE} = V_{CES}$, $T_j = 25 (125)^\circ\text{C}$		0,1	0,3	mA
$V_{CE(TO)}$	$T_j = 25 (125)^\circ\text{C}$		1,1 (1,1)	1,25 (1,25)	V
r_{CE}	$V_{GE} = 15 \text{ V}$, $T_j = 25 (125)^\circ\text{C}$		13,3 (17,3)	16 (21,3)	m Ω
$V_{CE(sat)}$	$I_{Cnom} = 75 \text{ A}$, $V_{GE} = 15 \text{ V}$, chip level		2,1 (2,4)	2,45 (2,85)	V
C_{ies}	under following conditions		5	6,6	nF
C_{oes}	$V_{GE} = 0$, $V_{CE} = 25 \text{ V}$, $f = 1 \text{ MHz}$		0,72	0,9	nF
C_{res}			0,38	0,5	nF
L_{CE}				30	nH
$R_{CC'+EE'}$	res., terminal-chip $T_c = 25 (125)^\circ\text{C}$		0,75 (1)		m Ω
$t_{d(on)}$	$V_{CC} = 600 \text{ V}$, $I_{Cnom} = 75 \text{ A}$		80		ns
t_r	$R_{Gon} = R_{Goff} = 10 \Omega$, $T_j = 125^\circ\text{C}$		45		ns
$t_{d(off)}$	$V_{GE} = \pm 15 \text{ V}$		430		ns
t_f			55		ns
$E_{on} (E_{off})$			11 (9)		mJ
Inverse diode					
$V_F = V_{EC}$	$I_{Fnom} = 75 \text{ A}$; $V_{GE} = 0 \text{ V}$; $T_j = 25 (125)^\circ\text{C}$		2 (1,8)	2,5	V
$V_{(TO)}$	$T_j = 125 ()^\circ\text{C}$		1,1	1,2	V
r_T	$T_j = 125 ()^\circ\text{C}$			15	m Ω
I_{RRM}	$I_{Fnom} = 75 \text{ A}$; $T_j = 125 ()^\circ\text{C}$		42		A
Q_{rr}	$di/dt = 800 \text{ A}/\mu\text{s}$		9,1		μC
E_{rr}	$V_{GE} = V$				mJ
Thermal characteristics					
$R_{th(j-c)}$	per IGBT			0,18	K/W
$R_{th(j-c)D}$	per Inverse Diode			0,5	K/W
$R_{th(c-s)}$	per module			0,05	K/W
Mechanical data					
M_s	to heatsink M6	3		5	Nm
M_t	to terminals M5	2,5		5	Nm
w				160	g







This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX.

This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee expressed or implied is made regarding delivery, performance or suitability.