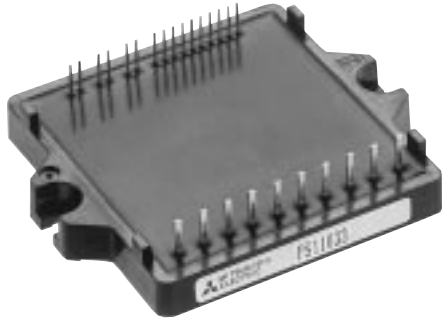




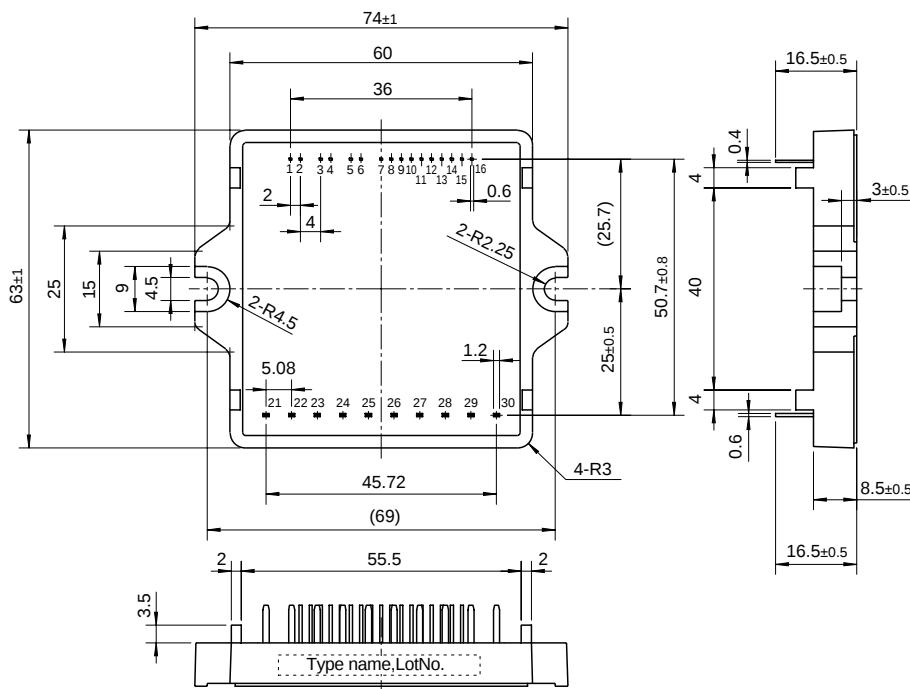
- Converter bridge for 3 phase AC-to-DC power conversion.
- 3 phase IGBT inverter bridge configured by the latest 3rd. generation IGBT and diode technology.
- Inverter output current capability I_o (Note 1):

Type Name	Motor Rating	Io (100%)	Io (150%; 60sec)
PS11033	0.4 kW/200V AC	3.0Arms	4.5Arms

(Note 1) : The inverter output current is assumed to be sinusoidal and the peak current value of each of the above loading cases is defined as : $I_{OP} = I_o \times \sqrt{2}$, $T_C < 100^\circ\text{C}$

- P-Side IGBTs : Drive circuit, high-level-shift circuit, bootstrap circuit supply scheme for Single Control-Power-Source drive, and under voltage (UV) protection.
- N-Side IGBTs : Drive circuit, DC-Link current sense and amplifier circuits for overcurrent protection, control-supply under-voltage protection (UV), and fault output (Fo) signaling circuit.
- Fault Output : N-side IGBT short circuit (SC), over-current (OC), and control supply under-voltage (UV).
- Inverter Analog Current Sense : N-Side IGBT DC-Link Current Sense.
- Input Interface : 5V CMOS/TTL compatible, Schmitt Trigger input, and Arm-Shoot-Through interlock protective function.

Acoustic noise-less 0.4kW/200V AC Class 3 phase inverters, motor control applications, and motors with built-in small size inverter package

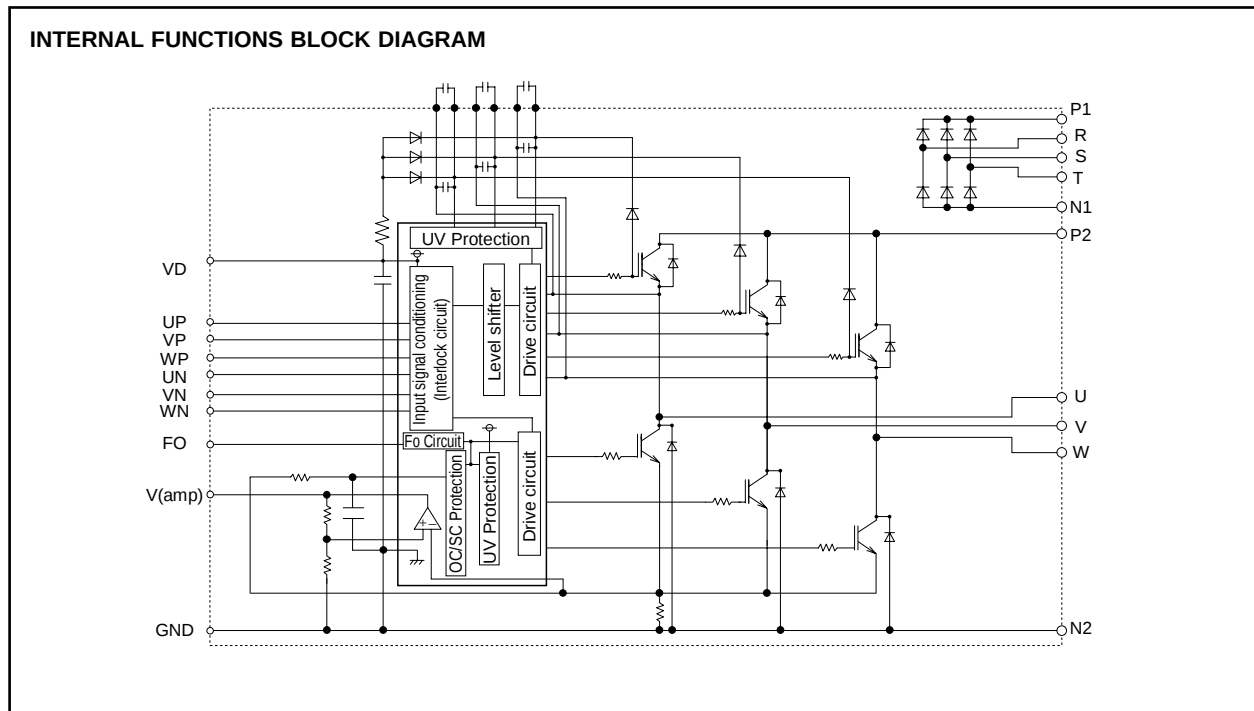


1. CBU+
2. CBU−
3. CBV+
4. CBV−
5. CBW+
6. CBW−
7. VD
8. UP
9. VP
10. WP
11. UN
12. VN
13. WN
14. FO
15. Vamp
16. GND
21. P1
22. R
23. S
24. T
25. N1
26. P2
27. U
28. V
29. W
30. N2

(Fig. 1)

PS11033

FLAT-BASE TYPE
INSULATED TYPE



(Fig. 2)

MAXIMUM RATINGS (Tj = 25°C)

INVERTER PART

Symbol	Item	Condition	Ratings	Unit
VCC	Supply voltage	Applied between P2-N2	450	V
VCC(surge)	Supply voltage (surge)	Applied between P2-N2, Surge-value	500	V
VP or VN	Each output IGBT collector-emitter static voltage	Applied between P2-U.V.W, U.V.W-N2	600	V
VP(S) or VN(S)	Each output IGBT collector-emitter switching voltage	Applied between P2-U.V.W, U.V.W-N2	600	V
±Ic(±Icp)	Each output IGBT collector current	Tc = 25°C, "()" means Ic peak value	±8 (±16)	A

CONVERTER PART

Symbol	Item	Condition	Ratings	Unit
VRRM	Repetitive peak reverse voltage		800	V
Ea	Recommended AC input voltage		220	Vrms
Io	DC output current	3φ rectifying circuit	10	A
IFSM	Surge (non-repetitive) forward current	1 cycle at 60Hz, peak value non-repetitive	100	A
I ² t	I ² t for fusing	Value for one cycle of surge current	42	A ² s

CONTROL PART

Symbol	Item	Ratings	Unit
VD, VDB	Supply voltage	-0.5 ~ 20	V
Vcin	Input signal voltage	-0.5 ~ +7.5	V
VFO	Fault output supply voltage	-0.5 ~ +7.5	V
Ifo	Fault output current	15	mA
Iamp	DC-Link IGBT current signal Amp output current	1	mA

PS11033

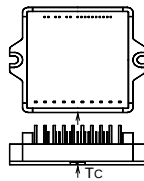
FLAT-BASE TYPE
INSULATED TYPE

TOTAL SYSTEM

Symbol	Item	Condition	Ratings	Unit
T _j	Junction temperature	(Note 2)	-20 ~ +125	°C
T _{stg}	Storage temperature	—	-40 ~ +125	°C
T _c	Module case operating temperature	(Fig. 3)	-20 ~ +100	°C
V _{iso}	Isolation voltage	60 Hz sinusoidal AC applied between all terminals and the base plate for 1 minute.	2500	Vrms
—	Mounting torque	Mounting screw: M4	0.98 ~ 1.47	N·m

(Note 2) : The indicated values are specified considering the safe operation of all the parts within the ASIPM. The max. ratings for the ASIPM power chips (IGBT & FWDi) is T_j < 150.

CASE TEMPERATURE MEASUREMENT POINT



(Fig. 3)

THERMAL RESISTANCE

Symbol	Item	Condition	Ratings			Unit
			Min.	Typ.	Max.	
R _{th(j)c} Q	Junction to case Thermal Resistance	Inverter IGBT (1/6)	—	—	4.1	°C/W
R _{th(j)c} F		Inverter FWDi (1/6)	—	—	6.1	°C/W
R _{th(j)c} FR		Converter Di (1/6)	—	—	4.8	°C/W
R _{th(cf)}	Contact Thermal Resistance	Case to fin thermal, grease applied (1 Module)	—	—	0.074	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C, V_D = 15V, V_{DB} = 15V unless otherwise noted)

Symbol	Item	Condition	Ratings			Unit
			Min.	Typ.	Max.	
V _{CE(sat)}	Collector-emitter saturation voltage	T _j = 25°C, Input = ON, I _c = 8A, V _D = V _{DB} = 15V (Shunt voltage drop not included)	—	—	2.9	V
V _{EC}	FWDi forward voltage	T _j = 25°C, -I _c = 8A	—	—	2.9	V
V _{FR}	Converter diode voltage	T _j = 25°C, I _{FR} = 5A	—	—	1.5	V
I _{RRM}	Converter diode reverse current	V _R = V _{RRM} , T _j = 125°C	—	—	8	mA
ton	Switching times	1/2 Bridge inductive, Input = 5V ↔ 0V V _{CC} = 300V, I _c = 8A, T _j = 125°C V _D = 15V, V _{DB} = 15V Note: ton, toff include delay time of the internal control circuit.	0.3	0.6	1.5	μs
tc(on)			—	0.43	0.8	μs
toff			—	1.6	2.5	μs
tc(off)			—	0.5	1.2	μs
trr	FWDi reverse recovery time		—	0.12	—	μs
Short circuit endurance (Output, Arm, and Load Short Circuit Modes)		@V _{CC} ≤ 400V, Input = 5V → 0V (One-Shot) -20°C ≤ T _j (start) ≤ 125°C, 13.5V ≤ V _D = V _{DB} ≤ 16.5V	- No destruction - Fo output by protection operation			
Switching SOA		@V _{CC} ≤ 400V, Input = 5V ↔ 0V, T _j ≤ 125°C I _c < OC trip level, 13.5V ≤ V _D = V _{DB} ≤ 16.5V	- No destruction - No protecting operation - No Fo output			

PS11033**FLAT-BASE TYPE
INSULATED TYPE****ELECTRICAL CHARACTERISTICS** ($T_j = 25^\circ\text{C}$, $V_D = 15\text{V}$, $V_{DB} = 15\text{V}$ unless otherwise noted)

Symbol	Item	Condition	Ratings			Unit
			Min.	Typ.	Max.	
I_D	Circuit current (Average)	$T_j = 25^\circ\text{C}$, $V_D = 15\text{V}$, $V_{in} = 5\text{V}$	—	—	50	mA
I_{DB}	Circuit current (Average)	$T_j = 25^\circ\text{C}$, $V_D = V_{DB} = 15\text{V}$, $V_{in} = 5\text{V}$	—	—	5	mA
$V_{th(on)}$	Input on threshold voltage		0.8	1.4	2.0	V
$V_{th(off)}$	Input off threshold voltage		2.5	3.0	4.0	V
R_i	Input pull-up resistor	Applied between input terminal-inside power supply	—	50	—	k Ω
f_{PWM}	PWM input frequency	$T_c \leq 100^\circ\text{C}$, $T_j \leq 125^\circ\text{C}$	1	—	15	kHz
t_{dead}	Arm shoot-through blocking time	Relates to corresponding inputs $T_c = -20^\circ\text{C} \sim +100^\circ\text{C}$ (Note 3)	2.2	—	—	μs
t_{int}	Input interlock sensing	Relates to corresponding input (Fig. 6)	—	100	—	ns
$V_{amp(100\%)}$	Inverter DC-Link IGBT current sense voltage	$I_c = I_{OP(100\%)}$ $V_D = 15\text{V}$	1.5	2.0	2.5	V
$V_{amp(200\%)}$	output signal	$I_c = I_{OP(200\%)}$ $T_j = 25^\circ\text{C}$ (Fig. 4)	3.0	4.0	5.0	V
$V_{amp(250\%)}$	Inverter DC-Link IGBT current sense voltage	$I_c = I_{OP(250\%)}$ $V_D = 15\text{V}$	5.0	—	—	V
$V_{amp(0)}$	output limit	$I_c = 0\text{A}$ (Fig. 4)	—	50	100	mV
OC	Over current trip level	$T_j = 25^\circ\text{C}$ (Fig. 5)	8.5	10.6	16.0	A
t_{OC}	Over current delay time	$T_j = 25^\circ\text{C}$ (Fig. 5)	—	10	—	μs
SC	Short circuit trip level	$T_j = 25^\circ\text{C}$ (Fig. 5)	—	16	—	A
t_{SC}	Short circuit delay time	$T_j = 25^\circ\text{C}$ (Fig. 5)	—	2	—	μs
UV_D	Supply circuit under voltage protection	Trip level	11.0	12.0	13.0	V
UV_{Dr}		Reset level	11.5	12.5	13.5	V
UV_{DB}		Trip level	10.1	10.8	11.6	V
UV_{DBr}		Reset level	10.6	11.3	12.1	V
tdV		Delay time	—	10	—	μs
t_{FO}	Fault output pulse width	$T_j = 25^\circ\text{C}$ (Note 4)	1.0	1.8	—	ms
$I_{FO(H)}$	Fault output current	Open collector output (Note 4)	—	—	1	μA
$I_{FO(L)}$			—	—	15	mA

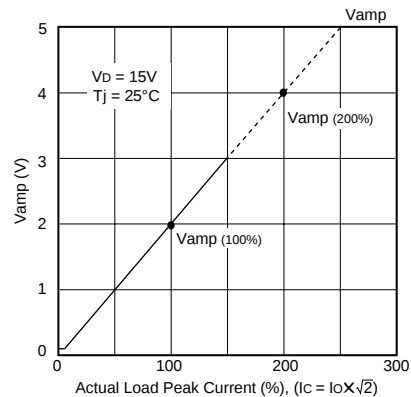
(Note 3) : The dead-time has to be set externally by the CPU; it is not part of the ASIPM internal functions.

(Note 4) : Fault output signaling is given only when the internal OC, SC, & UV protection circuits are activated.

The OC, SC and UV protection (and fault output) operate for the lower arms only. The OC and SC protection Fault output is given in a pulse format while that of UV protection is maintained throughout the duration of the under-voltage condition.

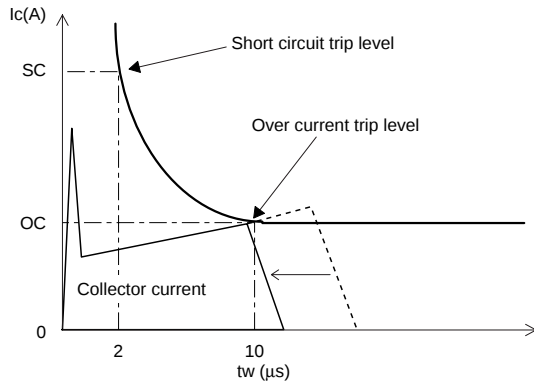
RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Condition	Ratings			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied across P2-N2 terminals	—	300	400	V
V_D	Supply voltage	Applied between V_D -GND	13.5	15.0	16.5	V
V_{DB}	Supply voltage	Applied between CBU+ & CBU-, CBV+ & CBV-, CBW+ & CBW-	13.5	15.0	16.5	V
$\Delta V_D, V_{DB}$	Supply voltage ripple		-1	—	+1	V/ μs
$V_{CIN(ON)}$	Input on voltage	Applied between UP • VP • WP • UN • VN • WN and GND	0	—	0.8	V
$V_{CIN(OFF)}$	Input off voltage		4.0	—	5.0	V
t_{dead}	Arm shoot-through blocking time	Relates to corresponding inputs	2.2	—	—	μs
T_c	Module case operating temperature		—	—	100	$^\circ\text{C}$
f_{PWM}	PWM Input frequency	$T_c \leq 100^\circ\text{C}$, $T_j \leq 125^\circ\text{C}$	—	—	15	kHz
t_{XX}	Allowable minimum input on-pulse width		1	—	—	μs

**INVERTER DC-LINK IGBT CURRENT ANALOGUE
SIGNaling OUTPUT (TYPICAL)**

(Fig. 4)

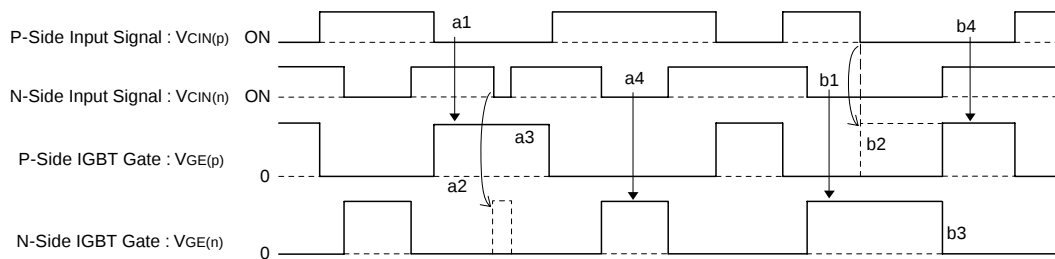
CURRENT ABNORMALITY PROTECTIVE FUNCTIONS



(Fig. 5)

Protection is achieved by monitoring and filtering the N-side DC-Bus current. The over-current protection is activated (after allowing a filtering time of 10 μ s) when the line current reaches 250% of the rated load-current I_o (rms). Similarly, the short circuit protection is activated (after allowing a filtering time of 2 μ s) when the line current reaches twice the rated collector-current (I_c). When a current trip-level is exceeded (OC or SC), all the N-side IGBTs are intercepted (turned OFF) and a fault-signal is output. After the fault-signal output duration (1.8 ms - typ.), the interception is Reset at the following OFF input signal. However, since the fault may be repetitive, it is recommended to stop the system after the fault-signal is received and check the fault. The trip-level settings described above are summarized in the following figure:

ARM-SHOOT-THROUGH INTER-LOCK PROTECTIVE FUNCTION



(Fig. 6)

Description:

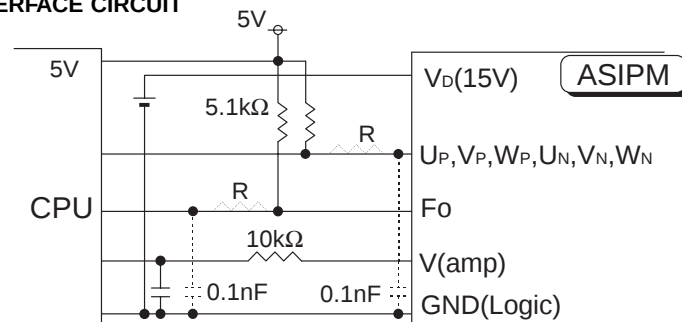
- (1) During the ON-State of either of the upper-arm or the lower-arm IGBT, the inter-lock protection circuit blocks any erroneous ON pulses (resulting from input noise) from triggering the other arm IGBT and thus it prevents the arm-shoot-through situation.
- (2) When two ON-signals are received for both the upper and the lower arms, the signal received first will be passed to the IGBT and the second signal will be blocked. The second signal will be passed to its corresponding IGBT immediately after the first signal is OFF.

Note: This protective function provides no fault signaling output. The Dead-Time has to be set using the micro-controller (CPU).

Operation:

- | | |
|---|--|
| a1. P-side normal ON-signal $\Rightarrow$ P-side IGBT gate turns ON. | b1. N-side normal ON-signal $\Rightarrow$ N-side IGBT gate turns ON. |
| a2. N-side erroneous ON-signal $\Rightarrow$ N-side IGBT gate remains OFF. | b2. Simultaneous ON-signals $\Rightarrow$ P-side IGBT gate remains OFF. |
| a3. While P-side ON-signal remains $\Rightarrow$ P-side IGBT gate remains ON. | b3. N-side receives OFF-signal $\Rightarrow$ N-side IGBT gate turns OFF. |
| a4. N-side normal ON-signal $\Rightarrow$ N-side IGBT gate turns ON. | b4. Immediately after (b3) $\Rightarrow$ P-side IGBT gate turns ON. |

RECOMMENDED I/O INTERFACE CIRCUIT



(Fig. 7)