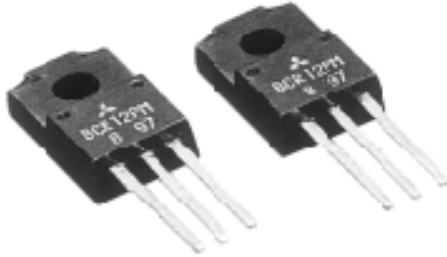


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MEDIUM POWER USE
INSULATED TYPE, PLANAR PASSIVATION TYPE

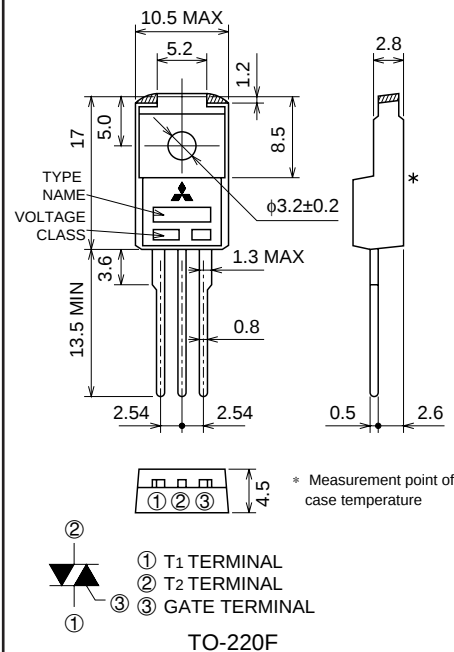
BCR12PM



- IT (RMS) 12A
- VDRM 400V/600V
- I_{FGT I}, I_{RGT I}, I_{RGT III} 30mA (20mA) *5
- V_{iso} 1500V
- UL Recognized: File No. E80276

OUTLINE DRAWING

Dimensions
in mm



APPLICATION

Switching mode power supply, light dimmer, electric flasher unit, hair driver,
control of household equipment such as TV sets · stereo · refrigerator · washing machine · infrared
kotatsu · carpet, solenoid drivers, small motor control,
copying machine, electric tool

MAXIMUM RATINGS

Symbol	Parameter	Voltage class		Unit
		8	12	
V _{DRM}	Repetitive peak off-state voltage *1	400	600	V
V _{DSM}	Non-repetitive peak off-state voltage *1	500	720	V

Symbol	Parameter	Conditions	Ratings	Unit
I_T (RMS)	RMS on-state current	Commercial frequency, sine full wave 360° conduction, $T_c=74^{\circ}\text{C}$	12	A
I_{TSM}	Surge on-state current	60Hz sinewave 1 full cycle, peak value, non-repetitive	120	A
I^2_t	I^2_t for fusing	Value corresponding to 1 cycle of half wave 60Hz, surge on-state current	60	A^2s
PGM	Peak gate power dissipation		5	W
PG (AV)	Average gate power dissipation		0.5	W
VGM	Peak gate voltage		10	V
IGM	Peak gate current		2	A
T_j	Junction temperature		$-40 \sim +125$	$^{\circ}\text{C}$
T_{stg}	Storage temperature		$-40 \sim +125$	$^{\circ}\text{C}$
—	Weight	Typical value	2.0	g
V_{iso}	Isolation voltage	$T_a=25^{\circ}\text{C}$, AC 1 minute, $T_1 \cdot T_2 \cdot G$ terminal to case	1500	V

*1. Gate open.

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MEDIUM POWER USE
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ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
IDRM	Repetitive peak off-state current	T _J =125°C, V _{DRM} applied	—	—	2.0	mA
V _{TM}	On-state voltage	T _C =25°C, I _{TM} =20A, Instantaneous measurement	—	—	1.6	V
V _{FGT} I	Gate trigger voltage *2	T _J =25°C, V _D =6V, R _L =6Ω, R _G =330Ω	—	—	1.5	V
V _{RGT} I			—	—	1.5	V
V _{RGT} III			—	—	1.5	V
I _{FGT} I	Gate trigger current *2	T _J =25°C, V _D =6V, R _L =6Ω, R _G =330Ω	—	—	30*5	mA
I _{RGT} I			—	—	30*5	mA
I _{RGT} III			—	—	30*5	mA
V _{GD}	Gate non-trigger voltage	T _J =125°C, V _D =1/2V _{DRM}	0.2	—	—	V
R _{th} (j-c)	Thermal resistance	Junction to case *4	—	—	3.5	°C/W
(dv/dt) _c	Critical-rate of rise of off-state commutating voltage		*3	—	—	V/μs

*2. Measurement using the gate trigger characteristics measurement circuit.

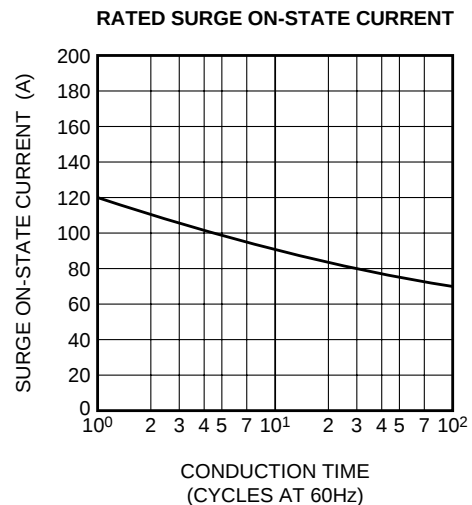
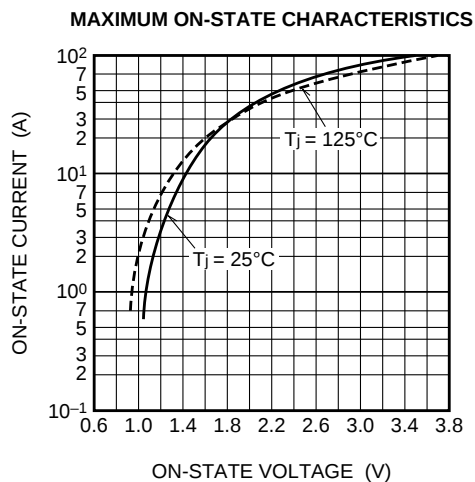
*3. The critical-rate of rise of the off-state commutating voltage is shown in the table below.

*4. The contact thermal resistance R_{th} (c-f) in case of greasing is 0.5°C/W.

*5. High sensitivity (I_{GT}≤20mA) is also available. (I_{GT} item ①)

Voltage class	V _{DRM} (V)	(dv/dt) _c			Test conditions	Commutating voltage and current waveforms (inductive load)
		Symbol	Min.	Unit		
8	400	R	—	V/μs	1. Junction temperature T _J =125°C 2. Rate of decay of on-state commutating current (di/dt) _c =-6.0A/ms 3. Peak off-state voltage V _D =400V	
		L	10			
12	600	R	—			
		L	10			

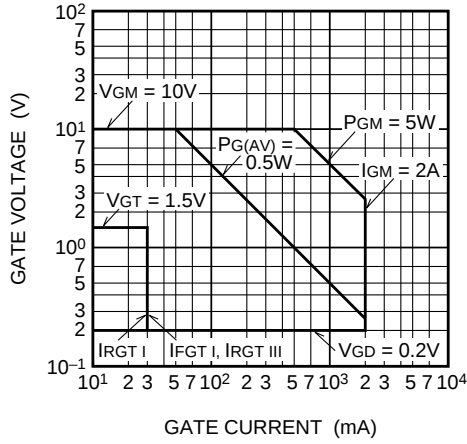
PERFORMANCE CURVES



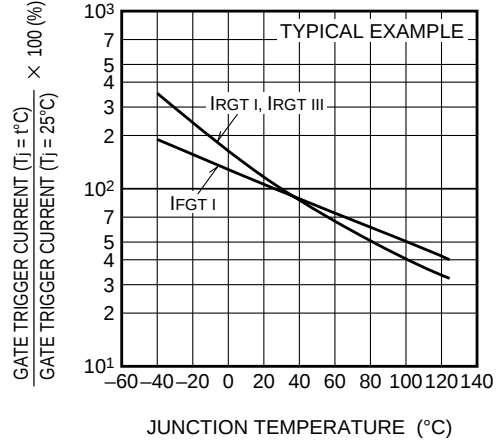
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MEDIUM POWER USE
INSULATED TYPE, PLANAR PASSIVATION TYPE

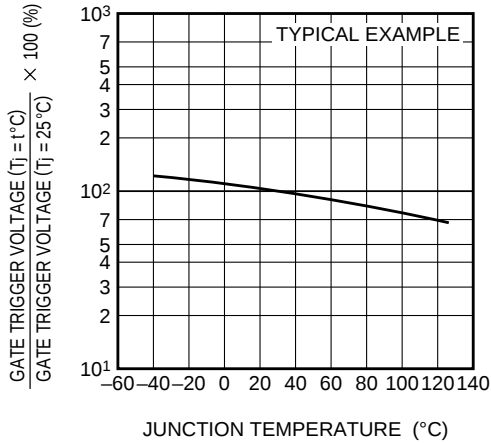
GATE CHARACTERISTICS



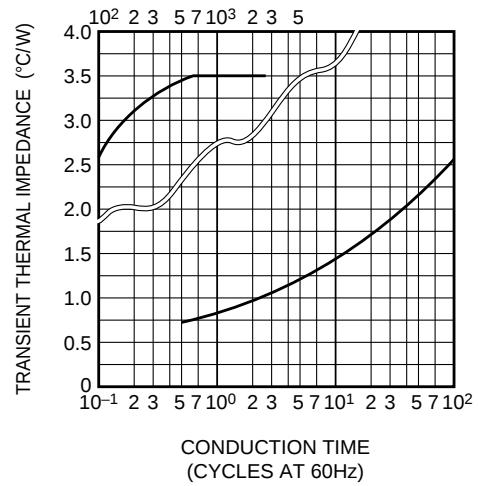
GATE TRIGGER CURRENT VS. JUNCTION TEMPERATURE



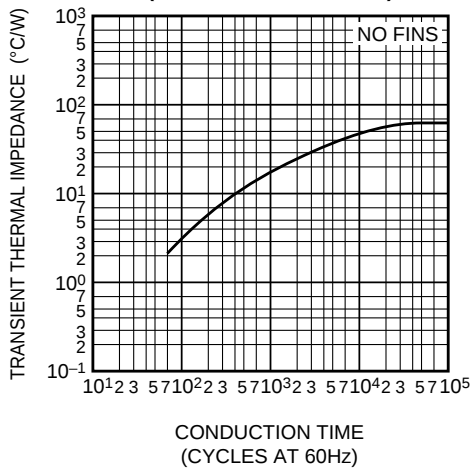
GATE TRIGGER VOLTAGE VS. JUNCTION TEMPERATURE



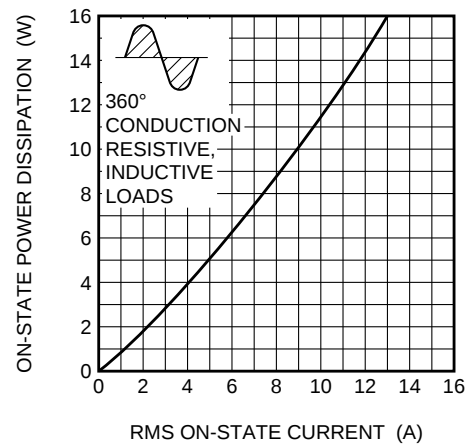
MAXIMUM TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (JUNCTION TO CASE)



MAXIMUM TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (JUNCTION TO AMBIENT)



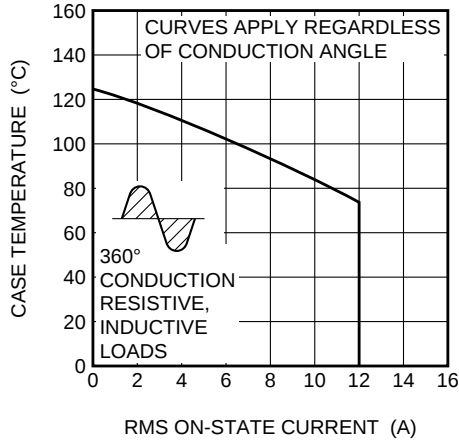
MAXIMUM ON-STATE POWER DISSIPATION



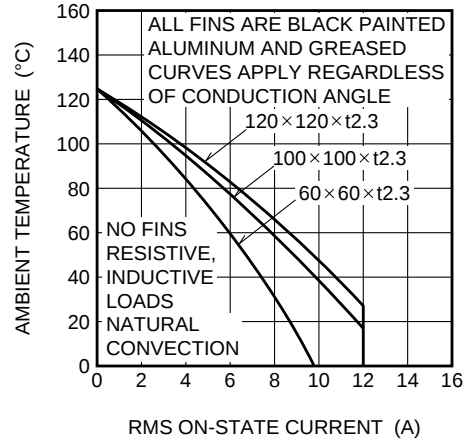
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MEDIUM POWER USE
INSULATED TYPE, PLANAR PASSIVATION TYPE

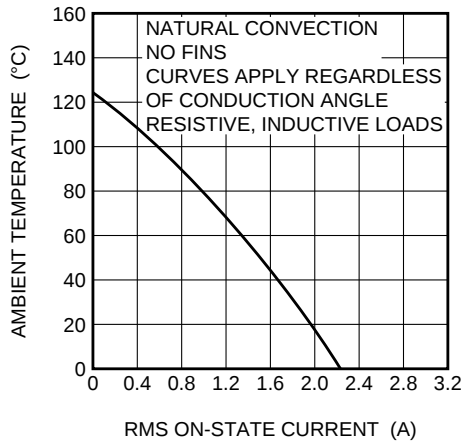
ALLOWABLE CASE TEMPERATURE
VS. RMS ON-STATE CURRENT



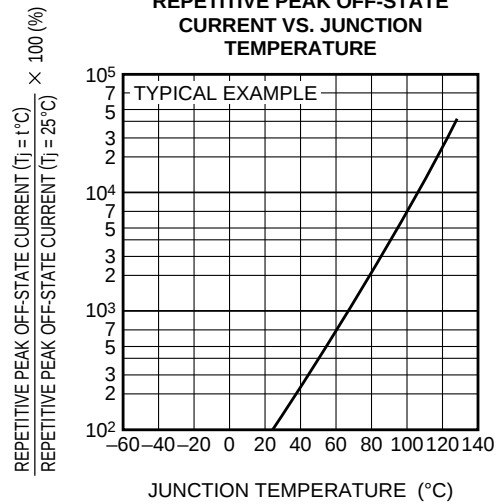
ALLOWABLE AMBIENT TEMPERATURE
VS. RMS ON-STATE CURRENT



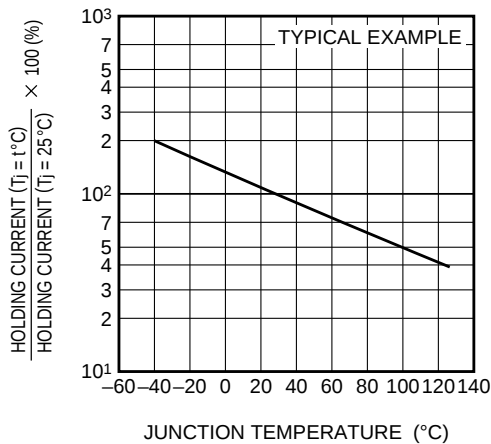
ALLOWABLE AMBIENT TEMPERATURE
VS. RMS ON-STATE CURRENT



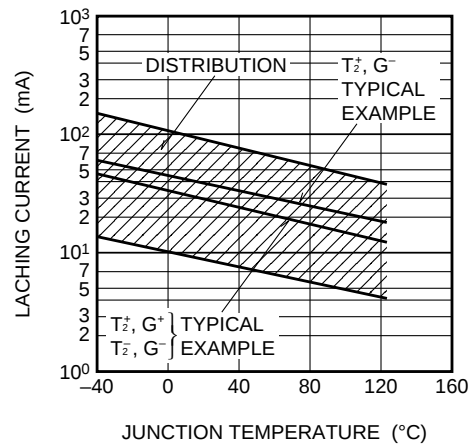
REPETITIVE PEAK OFF-STATE
CURRENT VS. JUNCTION
TEMPERATURE



HOLDING CURRENT VS.
JUNCTION TEMPERATURE

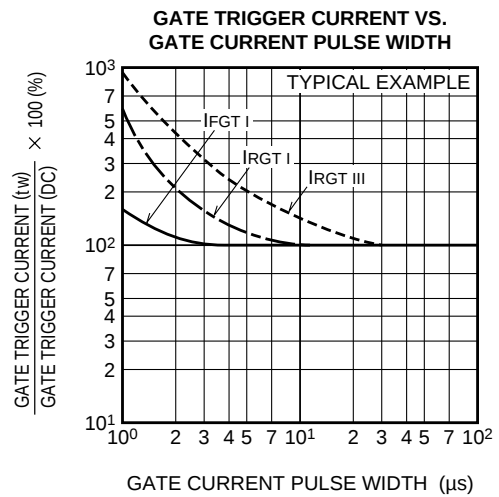
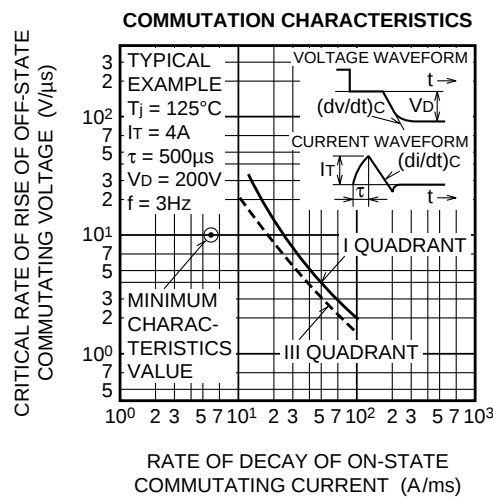
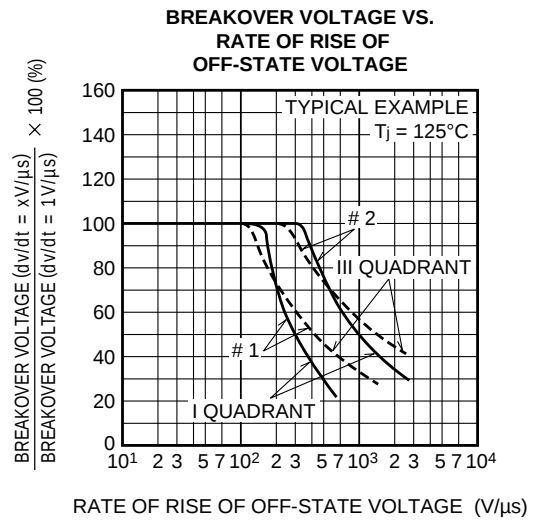
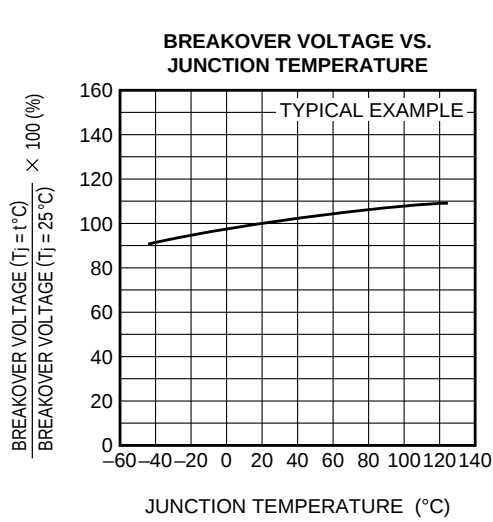


LACHING CURRENT VS.
JUNCTION TEMPERATURE



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MEDIUM POWER USE
INSULATED TYPE, PLANAR PASSIVATION TYPE



GATE TRIGGER CHARACTERISTICS TEST CIRCUITS

